# sensor to image

# CANCam-BF

## Smart camera with DSP, FPGA and CAN-Interface for demanding image processing in industry, medicine, research and security

**With increasing power of embedded processors, smart or intelligent camera systems become a reasonable alternative to PC-based imaging systems in various fields of application. CANCam-BF is a very powerful intelligent camera-system for advanced image processing independent from a host-PC.**



*CANCam-BF*

Heart of the intelligent camera platform is a BlackFin®-DSP running up to 600 MHz which was especially designed for signal and image processing tasks. This offers many possibilities to realize image processing inside the camera.

To provide a flexible and cost effective software platform, the open source operating system µClinux with GNU C/C++ compiler is used. Networking capabilities and fieldbus interface (CAN) of this system make development and connectivity easy.

In addition the *Sensor to Image Open FPGA-Technology* is introduced, which gives the vision application designer access to the Xilinx Spartan3 FPGA. This opens various additional possibilities, e.g. to write time critical image processing tasks to run in hardware.

This system is available with several CMOS or CCD linear/matrix imagers for monochrome or color imaging applications. To support other video sources like analog or CameraLink cameras or devices sending data in DVI or VGA format, several interface cards are available.

CANCAM-BF is a stand alone control unit. It can be integrated into existing Ethernet networks. So you can e.g. watch the camera image and configuration data by just opening your web browser. For advanced and secure systems you may prefer configuration by file. You can also load and store pictures, lookup tables or your

application software in the built in file system.

If the system fits not for 100% to your application, custom variants are welcome!
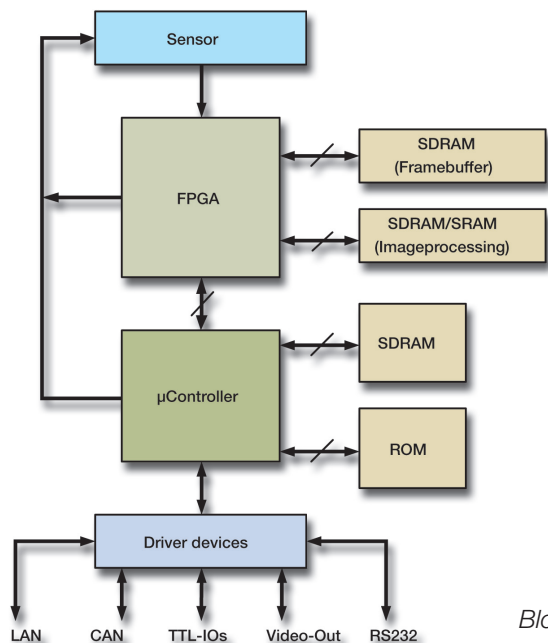


*Blockdiagram CANCam-BF*

## Complete Camera System

| | |
|---|---|
| CPU | BlackFin CPU Board |
| Video Interface AddOn | FPGA Sensor Interface |
| Sensor | CMOS/CCD imager |
| Power Supply | 8–24 V, 3 Watt |
| Dimensions Housing in mm | 56×46×99 |
| Lense Thread | C-Mount |

## CPU-System

| | |
|---|---|
| CPU | AD BF537/600 MHz @ 40°C / AD BF537/400 MHz @ > 40°C – 70°C |
| CPU Memory | 32 MByte, optional up to 64 MByte |
| Flash Memory | 8 MByte, optional up to 16 MByte |
| Operating System | µClinux Kernel 2.6 |
| RS232 / CAN Interface | 1/Yes |
| TTL-IOs | 2 inputs, 2 outputs, 1 GPIO |
| Image Processing Library | on demand |
| Power Supply | 8–24 V, 3 Watt |
| Dimensions PCB in mm | 75×50×17 |

## Available Sensor boards

| Sensor | 0460 | 0836M/C | 1323M/C | 1330M | 3015C | 2k15 |
|---|---|---|---|---|---|---|
| Sensor Type | CMOS matrix | CCD matrix | CCD matrix | CMOS matrix | CMOS matrix | CMOS linear |
| Monochrome/Color | m/c | m/c | m/c | m | c | m |
| Shutter | global | global | global | rolling | rolling | global |
| Pixel | 752×480 | 1024×768 | 1296×996 | 1280×1024 | 2048×1536 | 2048 |
| Pixel Size | 6 µm×6 µm | 4.65 µm×4.64 µm | 3.75 µm×3.75 µm | 5.2 µm×5.2 µm | 3.2 µm×3.2 µm | 7 µm×7 µm |
| Pixel Clock | 27 MHz | 20 MHz | 36 MHz | 48 MHz | 48 MHz | 30 MHz |
| Frames/s | 60 | 36 | 23 | 30 | 15 | 15000 |

Other sensors on request

## AddOn Modules

| | |
|---|---|
| FPGA Sensor Interface | ■ FPGA: Spartan3 –400 or –1000<br>■ Framebuffer: 8–32 MB SDRAM<br>■ Image Processing Memory: 8–32 MB SDRAM or 256 kB SRAM<br>■ Interface to Sensor to Image sensor boards<br>■ Dimension: 50×50×10 mm |
| CameraLink Interface | ■ One Base or Medium interface for CameraLink cameras<br>■ Pixelclock <=85MHz<br>■ FPGA: Spartan3A –700 or –1400<br>■ Image Processing Memory: 8–64 MB SDRAM<br>■ Dimension: 90×75×10 mm |
| DVI/VGA Interface | ■ DVI up to 1600×1200 @ 60 Hz – or –<br>■ VGA up to 170 MHz Pixelclock (e.g. 1920×1200 @ 60 Hz in 24 bit RGB)<br>■ FPGA: Spartan3A –700 or –1400<br>■ Image Processing Memory: 8–64 MB SDRAM<br>■ Dimension: 90×75×10 mm |